WHAT IS CLAIMED IS:

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- 1. A signal processing apparatus comprising:
 - an input circuit to receive an input signal;
- a feedforward equalizer comprising a high-pass filter and responsive to said input circuit; and
 - a decision feedback equalizer comprising:
 - a decision circuit responsive to said feed forward equalizer; and
 - a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.
 - 2. A signal processing circuit according to Claim 1, wherein said high-pass filter has a low outoff frequency.
 - 3. A signal processing circuit according to Claim 2, wherein said high-pass filter has a flat response.
- 4. A signal processing circuit according to Claim 1, wherein said high-pass filter has high attenuation at low frequency.
 - 5. A signal processing circuit according to Claim 1, wherein said high-pass filter has high attenuation at low frequencies.
 - 6. A signal processing circuit according to Claim 5, wherein the high attenuation is at least 20 db.
- 7. A signal processing circuit according to Claim 1, wherein said high-pass filter comprises a first finite impulse response filter (FIR).

- 8. A signal processing circuit according to Claim 7, wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI.
- 9. A signal processing circuit according to Claim 8, wherein each tap of said first 5 FIR filter has a corresponding doefficient W as follows:

$$W_0 = unity$$

$$0 < \sum_{i=1}^{M} W_{-i} + W_{o} + \sum_{i=1}^{n} W_{i} << 1$$
, and

$$\text{-1}{<<}W_1,\;\dots\;W_n<<0.$$

- 10. A signal processing circuit according to Claim 1, wherein said input circuit comprises an analog to digital converter.
- 11. A signal processing circuit according to Claim 1, wherein said decision circuit comprises a threshold circuit.
- 12. A signal processing circuit according to Claim 1, wherein said decision circuit comprises a Viterbi detector.
- 13. A signal processing circuit according to Claim 8, further comprising a first adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering.
 - 14. A signal processing circuit according to Claim 13, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.
- 20 15. A signal processing circuit according to Claim 13, wherein said first adaptive control circuit is operable only during signal acquisition.

- 16. A signal processing circuit according to Claim 1, wherein said feedback filter comprises a second finite impulse response filter (FIR).
- 17. A signal processing circuit according to Claim 15, further comprising a second adaptive control circuit to adapt taps of said second FIR.
- 5 18. A signal processing apparatus comprising:

input means for receiving an input signal;

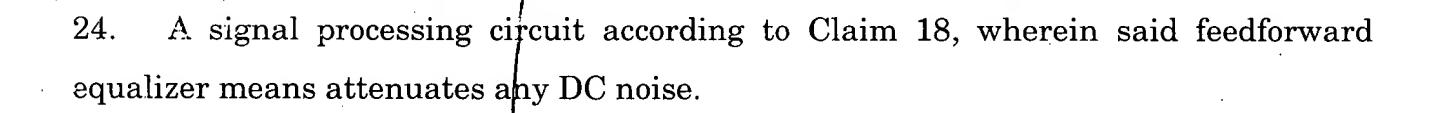
feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

- 19. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means has a low cutoff frequency.
- 20. A signal processing circuit according to Claim 19, wherein said feedforward equalizer means has a flat response.
- 21. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means has high attenuation at low frequency.
- 20 22. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means has high attenuation at low frequencies.
 - 23. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means shortens a length of postcursor inter-symbol interference.



- 25.A signal processing circuit according to Claim 18, wherein said feedforward equalizer means attenuates baseline wander.
- 26. A signal processing circuit according to Claim 22, wherein the high attenuation 5 is at least 20 db.
 - A signal processing circuit according to Claim 18, wherein said feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal.
 - 28. A signal processing circuit according to Claim 27, wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI.
 - A signal processing circuit according to Claim 28, wherein each tap of said first 29. FIR filter means has a corresponding coefficient W as follows:

$$W_0 = unity$$

$$0 < \sum_{1}^{M} W_{-i} + W_{o} + \sum_{1}^{n} W_{i} < 1$$
, and $-1 < < W_{1}, \dots W_{n} < < 0$.

$$-1 << W_1, \ldots W_n << 0.$$

- 30. A signal processing circuit according to Claim 18, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.
- A signal processing circuit according to Claim 18, wherein said decision means 31. comprises a threshold circuit.

- 32. A signal processing circuit according to Claim 18, wherein said decision means comprises a Viterbi detector.
- 33. A signal processing circuit according to Claim 28, further comprising a first adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering.
- 34. A signal processing circuit according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.
- 35. A signal processing circuit according to Claim 33, wherein said first adaptive control means is operable only during signal acquisition.
- 36. A signal processing circuit according to Claim 18, wherein said feedback filter means comprises a second finite impulse response filter (FIR) means for filtering the output of said decision means.
- 37. A signal processing circuit according to Claim 36, further comprising a second adaptive control means for adapting taps of said second FIR means.
- 15 38. An Ethernet transceiver, comprising:

an input for inputting an input signal into an Ethernet cable;

an output for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feed forward equalizer; and

- a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.
- 39. An Ethernet transceiver according to Claim 38, wherein said high-pass filter has a low cutoff frequency.
- 5 40. An Ethernet transceiver according to Claim 39, wherein said high-pass filter has a flat response.
 - 41. An Ethernet transceiver according to Claim 38, wherein said high-pass filter has high attenuation at low frequency.
 - 42. An Ethernet transceiver according to Claim 38, wherein said high-pass filter has high attenuation at low frequencies.
 - 43. An Ethernet transceiver according to Claim 42, wherein the high attenuation is at least 20 db.
 - 44. An Ethernet transceiver according to Claim 38, wherein said high-pass filter comprises a first finite impulse response filter (FIR).
- 45. An Ethernet transceiver according to Claim 44, wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI.
 - 46. An Ethernet transceiver according to Claim 45, wherein each tap of said first FIR filter has a corresponding coefficient W as follows:

$$w_0 = w_0$$

$$0 < \sum_{i=1}^{M} W_{-i} + W_o + \sum_{i=1}^{n} W_i << 1$$
, and

-1<<W1, ... Wn <<0.

- 47. An Ethernet transceiver according to Claim 38, wherein said input circuit comprises an analog to digital converter.
- 48. An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a threshold circuit.
- 49. An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a Viterbi detector.
- 50. An Ethernet transceiver according to Claim 45, further comprising a first adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering.
- 51. An Ethernet transceiver according to Claim 50, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.
- 52. An Ethernet transceiver according to Claim 50, wherein said first adaptive control circuit is operable only during signal acquisition.
- 15 53. An Ethernet transceiver according to Claim 38, wherein said feedback filter comprises a second finite impulse response filter (FIR).
 - 54. An Ethernet transceiver according to Claim 53, further comprising a second adaptive control circuit to adapt taps of said second FIR.
 - 55. A signal processing apparatus comprising:
- input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means; and

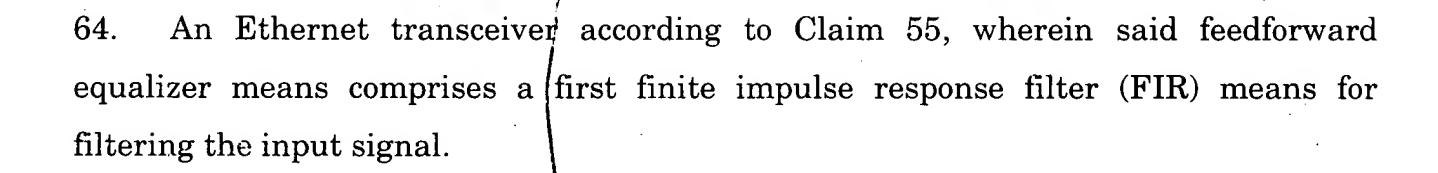
decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

- 56. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has a low cutoff frequency.
- 57. An Ethernet transceiver according to Claim 56, wherein said feedforward equalizer means has a flat response.
- 58. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has high attenuation at low frequency.
- An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has high attenuation at low frequencies.
- 60. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means shortens a length of postcursor inter-symbol interference.
- 61. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means attenuates any DC noise.
- 62. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means attenuates baseline wander.
- 20 63. An Ethernet transceiver according to Claim 59, wherein the high attenuation is at least 20 db.



- 65. An Ethernet transceiver according to Claim 64, wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI.
- 66. An Ethernet transceiver according to Claim 65, wherein each tap of said first FIR filter means has a corresponding coefficient W as follows:

$$W_0 = unity$$

$$0 < \sum_{i=1}^{M} W_{-i} + W_0 + \sum_{i=1}^{n} W_i << 1, \text{ and}$$

$$-1 << W_1, \dots W_n << 0.$$

- 67. An Ethernet transceiver according to Claim 55, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.
- 15 68. An Ethernet transceiver according to Claim 55, wherein said decision means comprises a threshold circuit.
 - 69. An Ethernet transceiver according to Claim 55, wherein said decision means comprises a Viterbi detector.
- 70. An Ethernet transceiver according to Claim 65, further comprising a first adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering.

- 71. An Ethernet transceiver according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.
- 72. An Ethernet transceiver according to Claim 70, wherein said first adaptive control means is operable only during signal acquisition.
- 5 73. An Ethernet transceiver according to Claim 55, wherein said feedback filter means comprises a second finite impulse response filter (FIR) means for filtering the output of said decision means.
 - 74. An Ethernet transceiver according to Claim 73, further comprising a second adaptive control means for adapting taps of said second FIR means.